Customer No.: 31561
Application No.: 10/707,867
Docket No.: 11870-US-PA

AMENDMENTS

Please amend the application as indicated hereafter.

To the Claims

Claims 1-9. (cancelled)

Claim 10. (currently amended) An analog-to-digital signal converter circuit, comprising:

a first capacitor, having a first terminal and a second terminal, wherein said first terminal is coupled to a first voltage level;

a clock generator, for generating a plurality of clock signals;

a switching capacitor network, coupled to said second terminal of said first capacitor, wherein the switching capacitor network receives an analog signal and said clock signals, said switching capacitor network stores a portion of charges of said analog signal, and outputs said portion of charges according to said clock signals to charge the first capacitor, and generates a threshold voltage associated with said first capacitor; and

a comparator, for comparing said threshold voltage with said analog signal and outputting a digital signal.

Claim 11. (original) The circuit of claim 10, wherein said switching capacitor network comprises:

a plurality of sensor control switches, wherein one of said sensor control switches is controlled by said clock signals for turning on/off, said sensor control switches are series-connected to form a series structure having a first terminal and a second terminal, said first terminal of said series structure receiving said analog signal and said second terminal of series

structure being coupled to said second terminal of said first capacitor so as to output said threshold voltage; and

at least a second capacitor, having a first terminal and a second terminal, said first terminal of said second capacitor being coupled to a connection between two adjacent sensor control switches in said series structure, said second terminal of said second capacitor being coupled to a second voltage level.

Claim 12. (original) The circuit of claim 11, wherein said of clock signals have a same frequency with different phases respectively.

Claim 13. (original) The circuit of claim 12, wherein said clock signals do not overlap.

Claim 14. (original) The circuit of claim 13, wherein said sensor control switches are MOSFETs.

Claim 15. (original) The circuit of claim 14, wherein said first voltage level and said second voltage level are DC voltage levels.

Claim 16. (original) The circuit of claim 10, wherein said circuit applies to a frequency-shift keying communication system.

Claim 17. (original) The circuit of claim 10, wherein said circuit applies to an amplitude-shift keying communication system.

Claim 18. (original) The circuit of claim 10, wherein said circuit applies to an on/off keying communication system.

Claim 19. (original) A method for converter an analog signal to a digital signal, comprising:

providing a first capacitor and a plurality of clock signals;

storing a portion of charges of an analog signal according to said clock signals;

generating a threshold voltage according to said clock signals based on said portion of charges associated with said first capacitor ; and

comparing said threshold voltage with said analog signal in order to output a digital signal.

Claim 20. (original) The method for converter of claim 19, wherein said clock signals comprises a first clock signal and a second clock signal, said first and second clock signals have a same frequency but not overlapping, and said step of generating said threshold voltage further comprising:

providing a second capacitor;

conducting said analog signal to said second capacitor according to said first clock signal to store said portion of charges of said analog signal in said second capacitor; and

conducting said first capacitor and said second capacitor in response to said second clock signal in order to generate said threshold voltage based on said portion of charges of said analog signal associated with said first capacitor.